Version: 1
Total Pages: 20
Date: 2004/3/10

Product Functional Specification

14.1 inch XGA Color TFT LCD Module
Model Name: B141XG08 V.3

( ) Preliminary Specification
(◆) Final Specification

Note: This Specification is subject to change without notice.

Contents

II Record of Revision

Version and Date	Page	Old description	New Description	Remark
V1. 2004/3/10	All	First Release	NA	

1.0 Handling Precautions

1) Do not press or scratch the surface harder than a HB pencil lead because the polarizers are very fragile and could be easily damaged.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water droplets or oil immediately. Long contact with the droplets may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Protect the module from static electricity and insure proper grounding when handling. Static electricity may cause damage to the CMOS Gate Array IC.
7) Do not disassemble the module.
8) Do not press the reflector sheet at the back of the module.
9) Avoid damaging the TFT module. Do not press the center of the CCFL Reflector when it was taken out from the packing container. Instead, press at the edge of the CCFL Reflector softly.
10) Do not rotate or tilt the signal interface connector of the TFT module when you insert or remove other connector into the signal interface connector.
11) Do not twist or bend the TFT module when installation of the TFT module into an enclosure (Notebook PC Bezel, for example). It should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside when designing the enclosure. Otherwise the TFT module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local regulations for disposal.
13) The LCD module contains a small amount of material that has no flammability grade, so it should be supplied by power complied with requirements of limited power source (2.11, IEC60950 or UL1950).
14) The CCFL in the LCD module is supplied with Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2.0 General Description

This specification applies to the 14.1 inch Color TFT/LCD Module B141XG08 V3

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

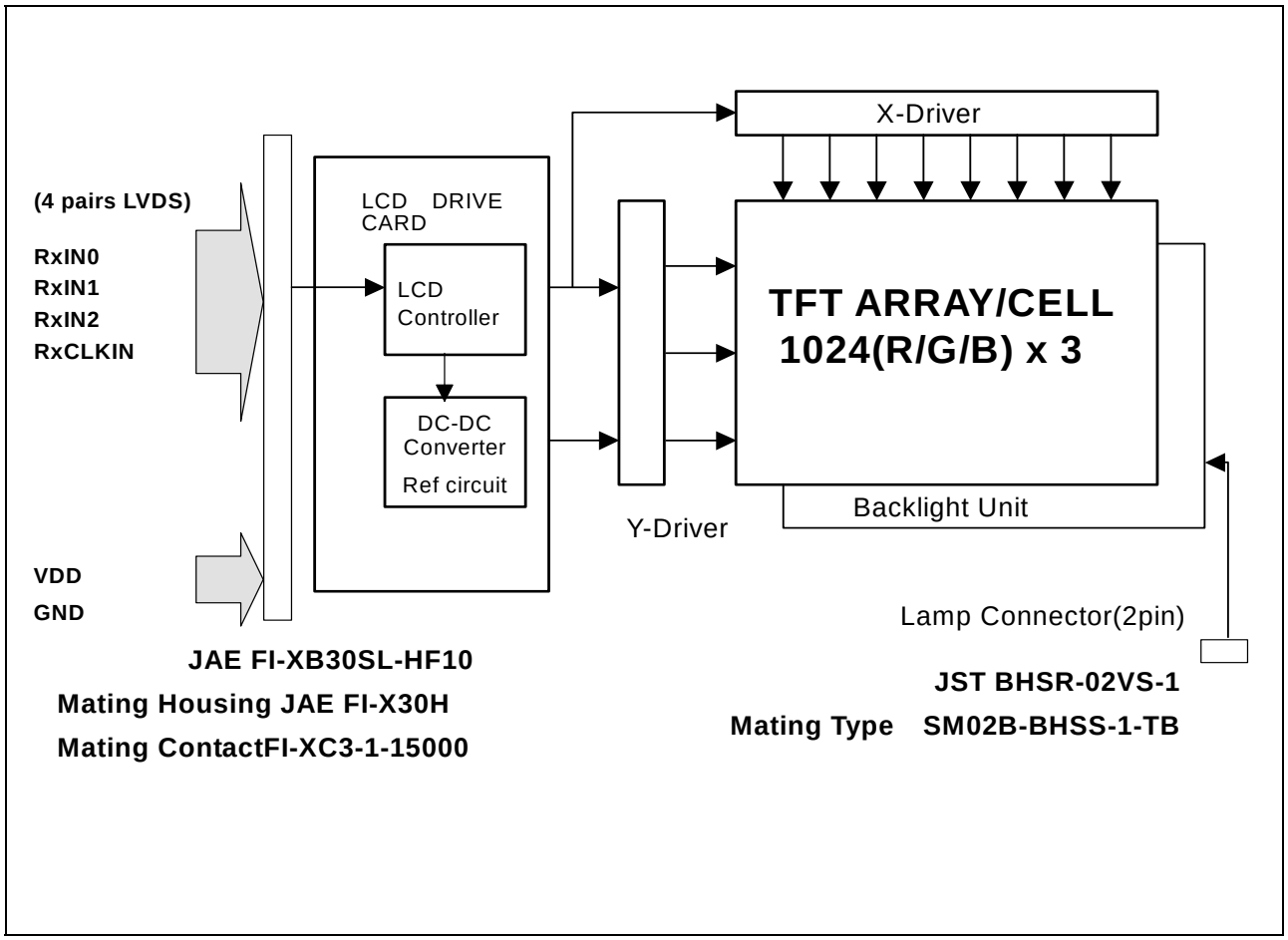
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	357(14.1")
Active Area	[mm]	285.7(H) x 214.3(V)
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.279(per one triad) x 0.279
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance(CCFL=6.0mA)	[cd/m^2]	200 Typ.(5 points average)
Contrast Ratio		250 : 1 Min ,300:1 Typ
ResponseTime	[msec]	25 Typ.
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	5.3 Watt (w/o Inverter, All black pattern)@LCM circuit 1.4 Watt(typ.),B/L input 3.9 Watt(typ.)
Weight	[Grams]	420g Max. (w/o Inverter)
Physical Size	[mm]	299(W) x 228(H) x 5.5(D) Max.
Electrical Interface		R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS)
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [^{o}C] [^{o}C]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

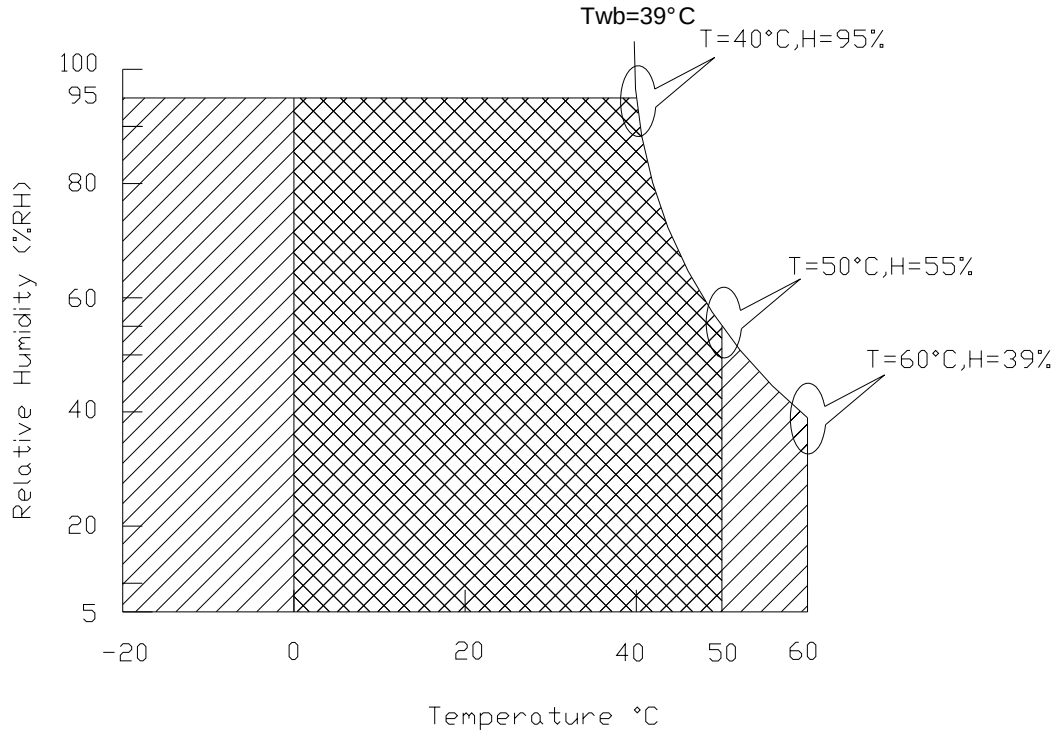
Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1160(25°C)	Vrms	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	5	95	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	5	95	[%RH]	Note 2
Vibration			2.16 10-500	[G Hz]	
Shock			240 , 2	[G ms]	Half sine wave

Note 1 : Duration = 50msec

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

Wet bulb temperature chart



Operating Range

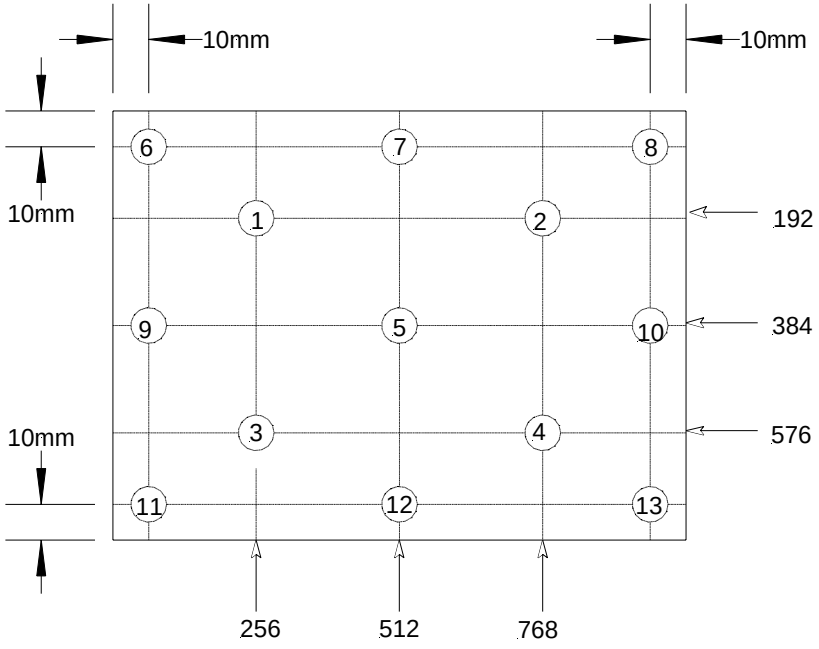
Storage Range

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	40 40	- -	- -	3,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	10 30	- -	- -	
Uniformity		5 Points			1.2	2
Uniformity		13 Points			1.5	
Contrast ratio			250	300	-	6
Response Time	[msec]	Rising	-	10	15	5
	[msec]	Falling	-	15	20	
Color / Chromaticity Coordinates (CIE)		Red x	0.57	0.600	0.63	3,7
		Red y	0.31	0.340	0.37	
		Green x	0.28	0.310	0.34	
		Green y	0.53	0.560	0.59	
		Blue x	0.12	0.150	0.18	
		Blue y	0.10	0.130	0.16	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
White Luminance CCFL 6.0mA	[cd/m^2]	5 points average	170	200	-	1,3,4

Note 1: 5 & 13 points position (Display area : 285.7mm x 214.3)



Note 2: Definition of white uniformity:

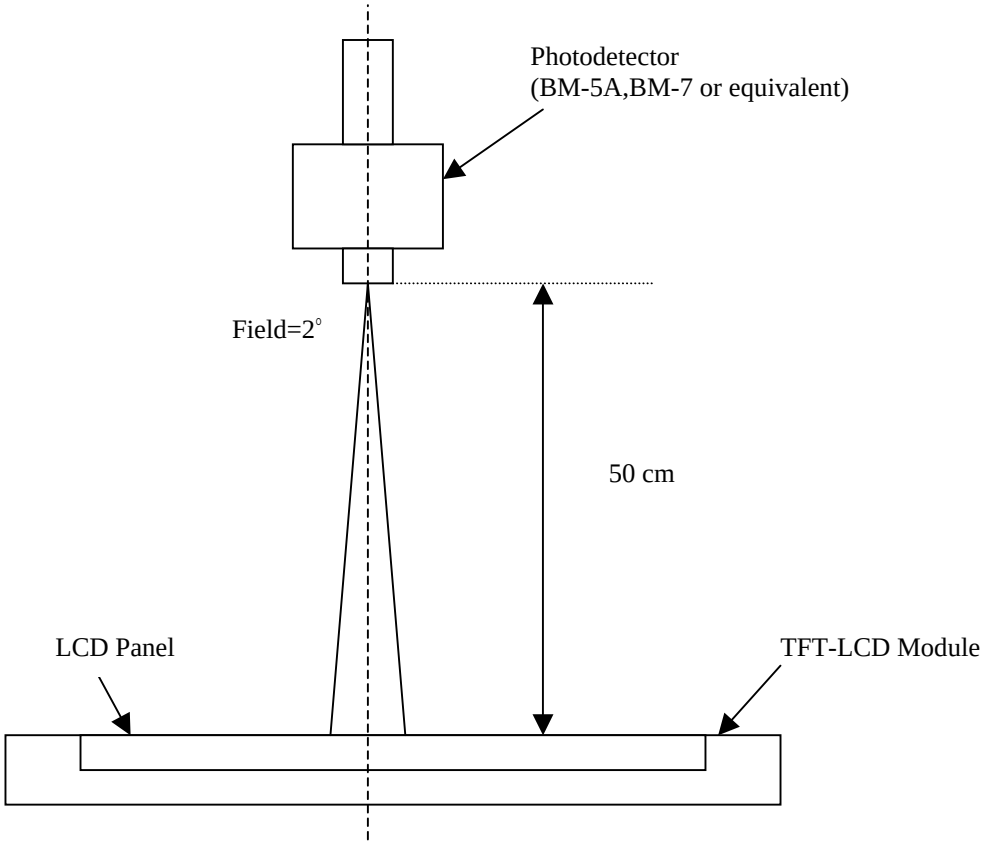
White uniformity is defined as the following with five/thirteen measurements (1~13) at Figure in Note (1). .

$$\delta_{W5} = \frac{\text{Maximum Brightness of five (1,2,3,4,5) points}}{\text{Minimum Brightness of five (1,2,3,4,5) points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 3: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Center of the screen

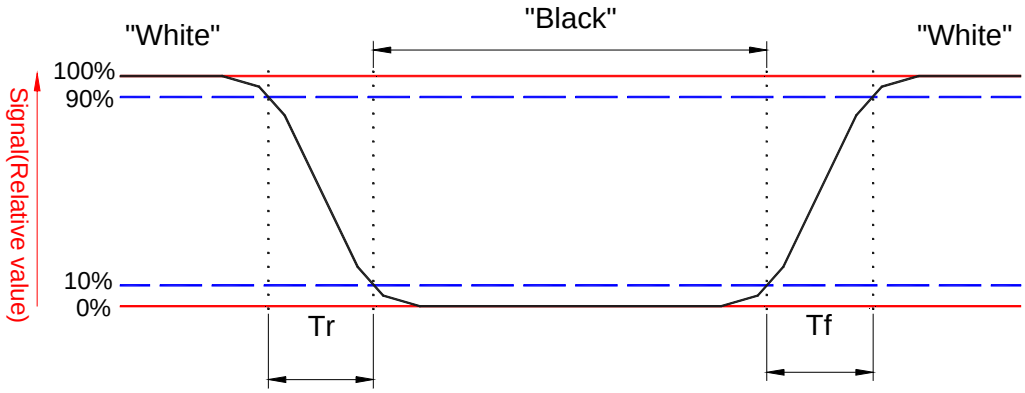
Note 4: Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points, Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 5: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



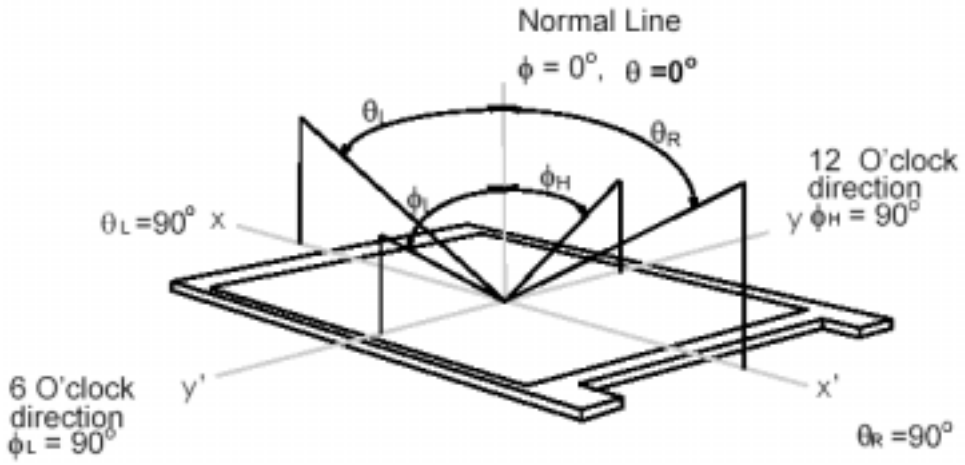
Note 6. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Housing/Part Number	FI-X30H
Mating Contact/Part Number	FI-XC3-1-15000

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	V_{EDID}
5	NC	6	CLK_{EDID}
7	$DATA_{EDID}$	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20~30	NC

5.3 Signal Description

The module uses a LVDS receiver embedded in AUO's ASIC. LVDS is a differential signal technology for LCD interface and high-speed data transfer device.

Signal Name	Description
V_{EDID}	+3.3V EDID Power
CLK_{EDID}	EDID Clock Input
$DATA_{EDID}$	EDID Data Input
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be in low status when VDD is off.

Internal circuit of LVDS inputs are as following.

Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

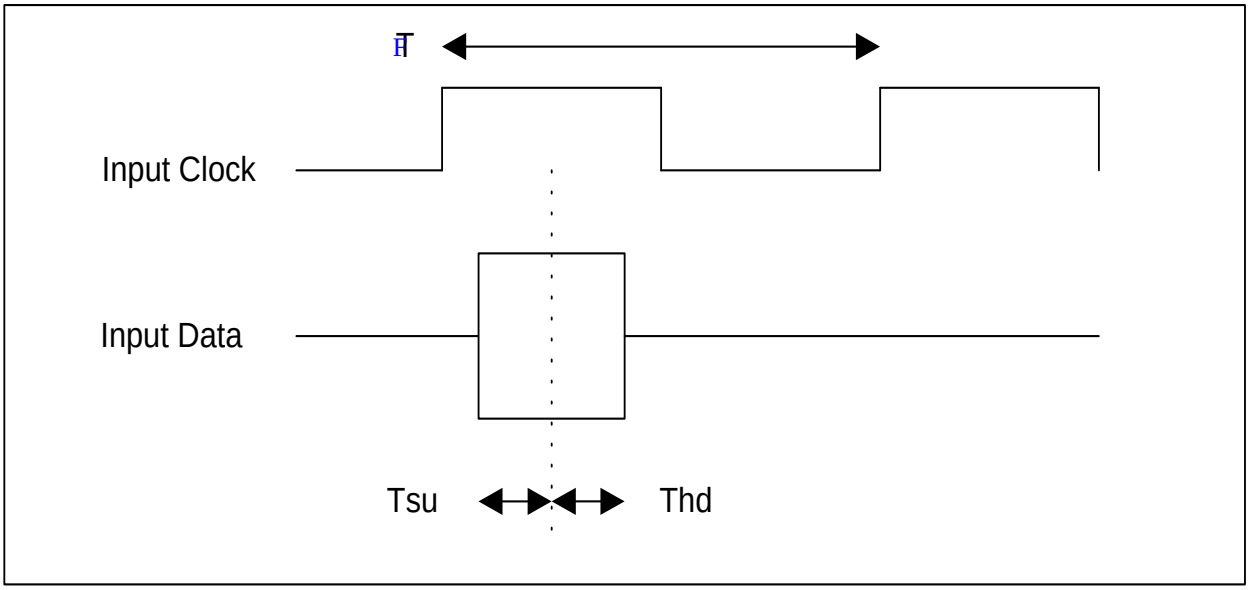
5.4 Signal Electrical Characteristics

Input signals shall be in low status when VDD is off.
It is recommended to refer the specifications of SN75LVDS86DGG (Texas Instruments) in detail.
Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage(Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Voltage(Vcm=+1.2V)	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (F)	50MHz	67MHz
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	

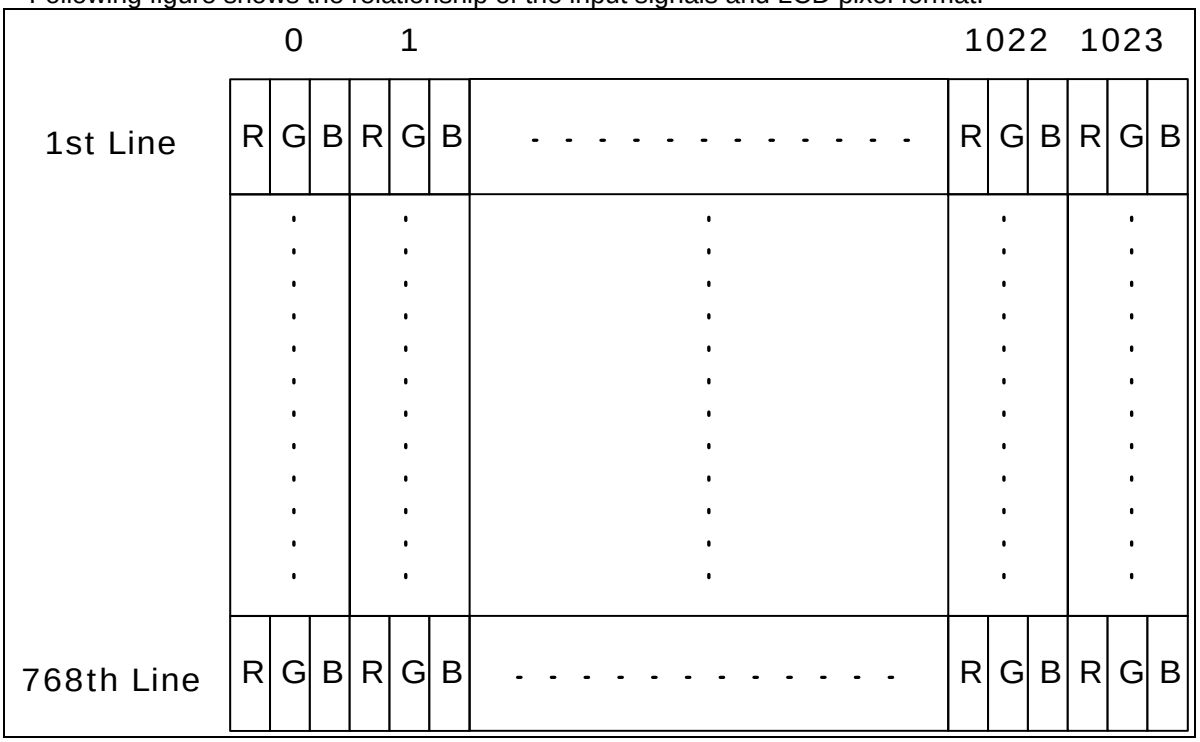


5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CCFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	170	200	—	[cd/m^2]	(Ta=25°C)
CCFL current(ICFL)		6.0	7.0	[mA] rms	(Ta=25°C) **Note 2**
CCFL Frequency(FCFL)	50	60	70	[KHz]	(Ta=25°C) **Note 3**
CCFL Ignition Voltage(Vs)		—	1500	[Volt] rms	(Ta= 0°C) **Note 4**
CCFL Voltage (Reference) (VCFL)	—	650	—	[Volt] rms	(Ta=25°C) **Note 5**
CCFL Power consumption (PCFL)	—	3.9	—	[Watt]	(Ta=25°C) **Note 5**

Note 1: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
*4 Generally, CCFL has some amount of delay time after applying start-up voltage. It is recommended to keep on applying start-up voltage for 1 [Sec] until discharge.
*5 The CCFL inverter operating frequency must be carefully chosen so that no interfering noise stripes on the screen were induced.
*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter, which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: The CCFL inverter operating frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The inverter open voltage should be designed larger than the lamp starting voltage at T=0^{o}C, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage. for longer than 1 second even if lamp connector is open.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

8.0 Interface Timings

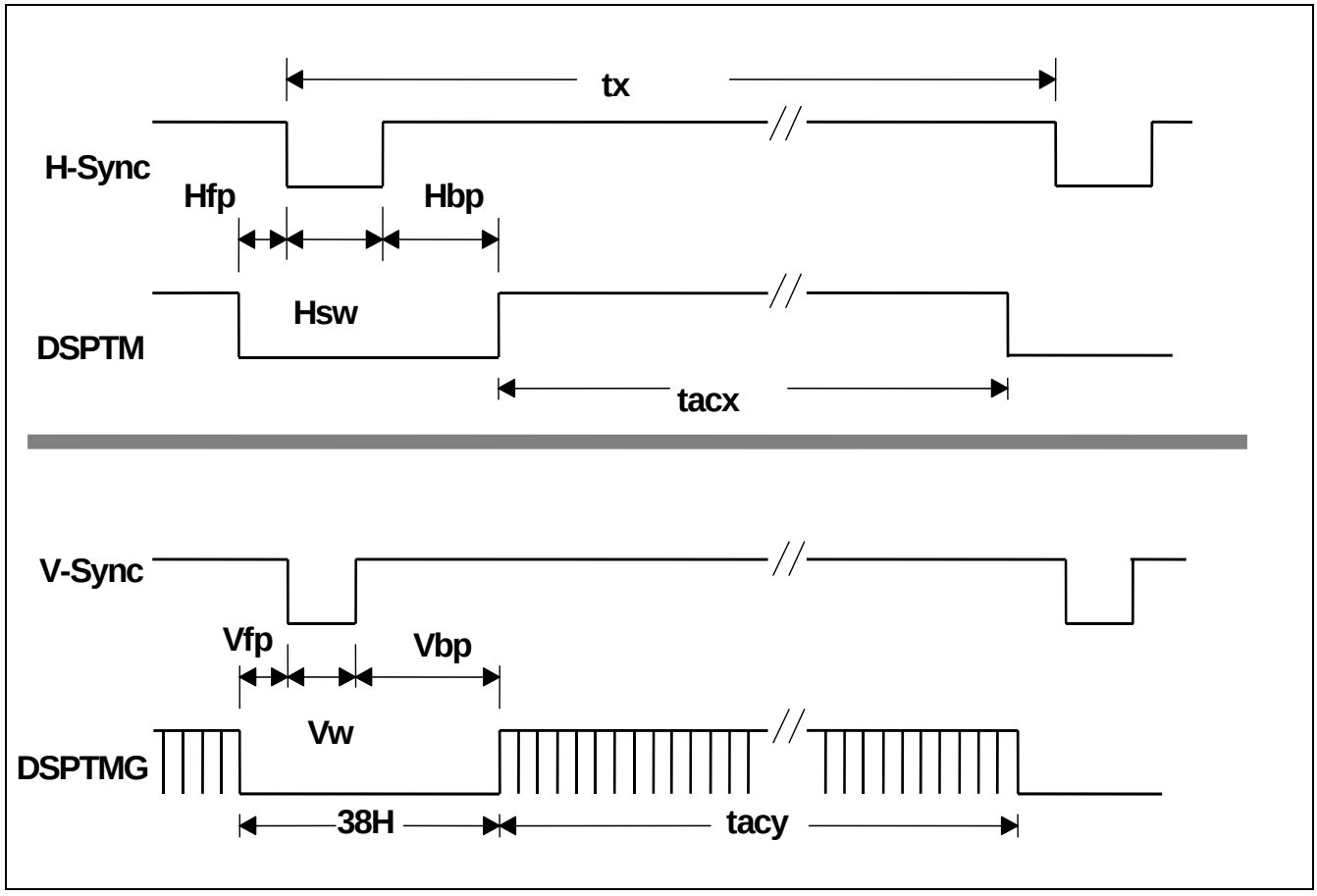
Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency		65.00		[MHz]
tck	DTCLK cycle time		15.38		[nsec]
tx	X total time	1206	1344	2047	[tck]
tacx	X active time	129	1024		[tck]
tbkx	X blank time	90	320		[tck]
Hsync	H frequency		48.363		[KHz]
Hsw	H-Sync width	2	136		[tck]
Hbp	H back porch	1	160		[tck]
Hfp	H front porch	0	24		[tck]
ty	Y total time	771	806	1023	[tx]
tacy	Y active time		768		[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
Vw	V-sync Width	1	6		[tx]
Vfp	V-sync front porch	1	3		[tx]
Vbp	V-sync back porch	7	29	63	[tx]

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition



9.0 Power Consumption

Input power specifications are as follows;

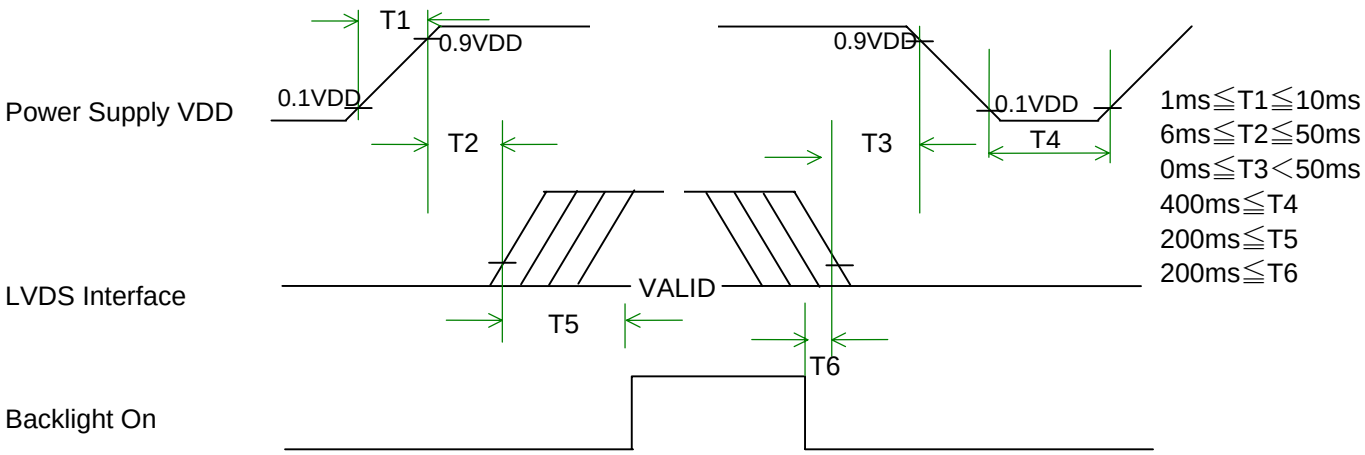
Symbol	Parameter	Min	Typ	Max	Units	Condition
Module						
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.4		[Watt]	All Black Pattern
PDD Max	VDD Power max			1.65	[Watt]	Max Pattern **Note**
IDD	IDD Current		350		mA	64 Grayscale Pattern
IDD Max	IDD Current max			450	mA	Vertical stripe line Pattern **Note**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	
Lamp						
ICFL	CCFL current	3.0	6.0	7.0	[mA] rms	(Ta=25°C)
VCFL	CCFL Voltage (Reference)	—	650	—	[Volt] rms	(Ta=25°C)
PCFL	CCFL Power consumption	—	3.9	—	[Watt]	(Ta=25°C)
Total Power Consumption	5.3 Watt (w/o Inverter, All black pattern)@LCM circuit 1.4 Watt(typ.),B/L input 3.9 Watt(typ.)					

Note : VDD=3.3V

10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

Sequence of Power-on/off and signal-on/off



Apply the lamp voltage within the LCD operating range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal.

11.0 Reliability /Safety Requirement

11.1 Reliability Test Conditions

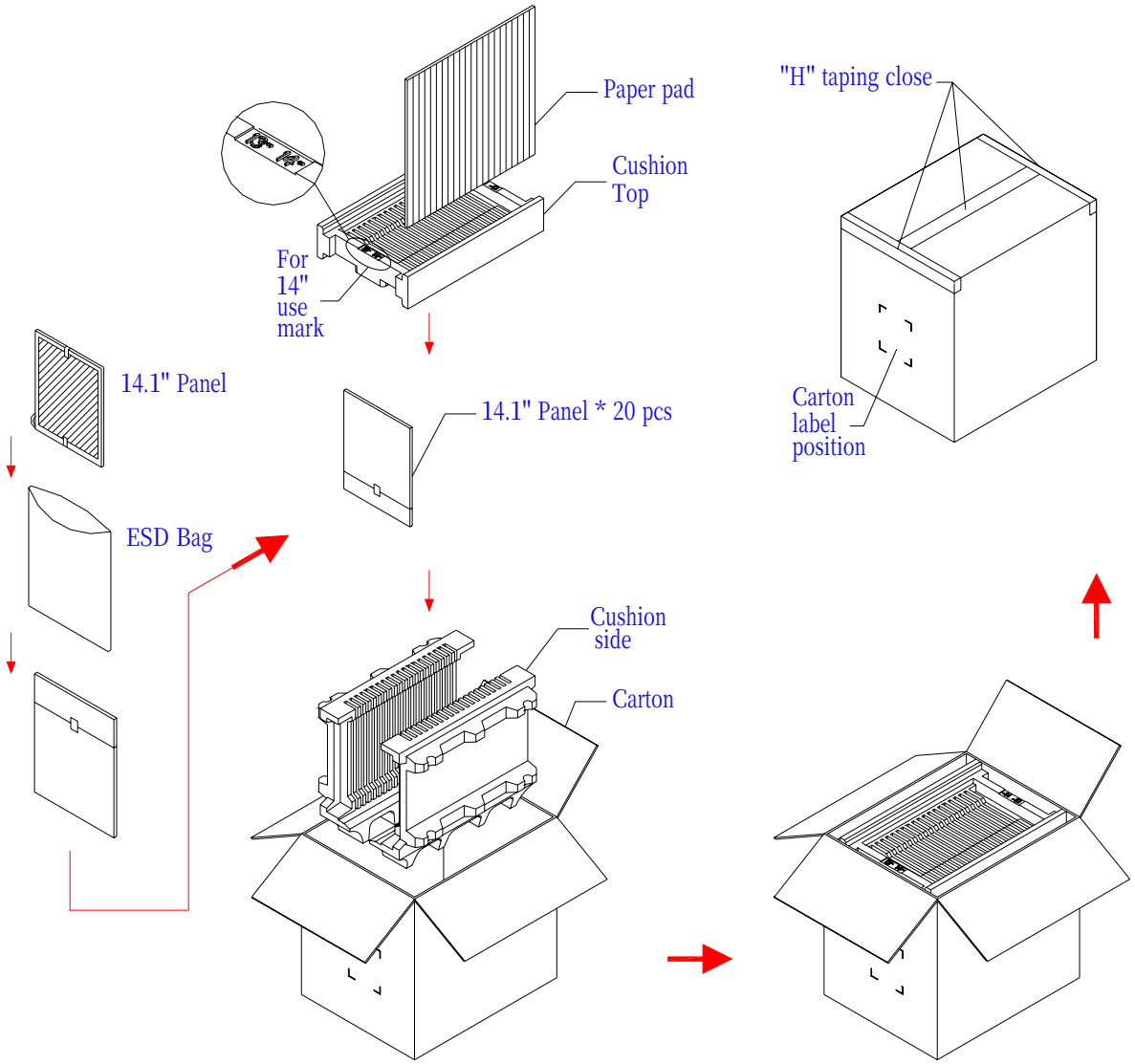
Items	Required Condition
Temperature Humidity Bias	40℃/90%,300Hr
High Temperature Operation	50℃/Dry,300Hr
Low Temperature Operation	0℃,500Hr
Continuous Life	25℃ ,2000 hours
On/Off Test	ON/30 sec. OFF/30sec., 30,000 cycles
Hot Storage	60℃/40% RH ,240 hours
Cold Storage	-20℃/50% RH ,240 hours
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times
Shock Test (Non-Operating)	240G, 2ms, Half-sine wave
Vibration Test (Non-Operating)	Sinusoidal vibration, 1.5G zero-to-peak, 10 to 500 Hz, 0.5 octave/minute; 0.5hr in each of three mutually perpendicular axes.
ESD	Contact : operation ±8KV / non-operation ±10KV Air : operation ±15KV / non-operation ±20KV
Altitude Test	10000 ft / operation / 8Hr 30000ft / non-operation / 24r
Maximum Side Mount Torque	2.5kgf.cm .

CCFL Life : 10,000 hours minimum
MTBF(Excluding the CCFL) : 30,000 hours with a confidence level 90%

11.2 Safety

UL 60950

12.0 Packing dimension



13.0 Mechanical Characteristics

13.1 LCM Outline dimension (Front View)

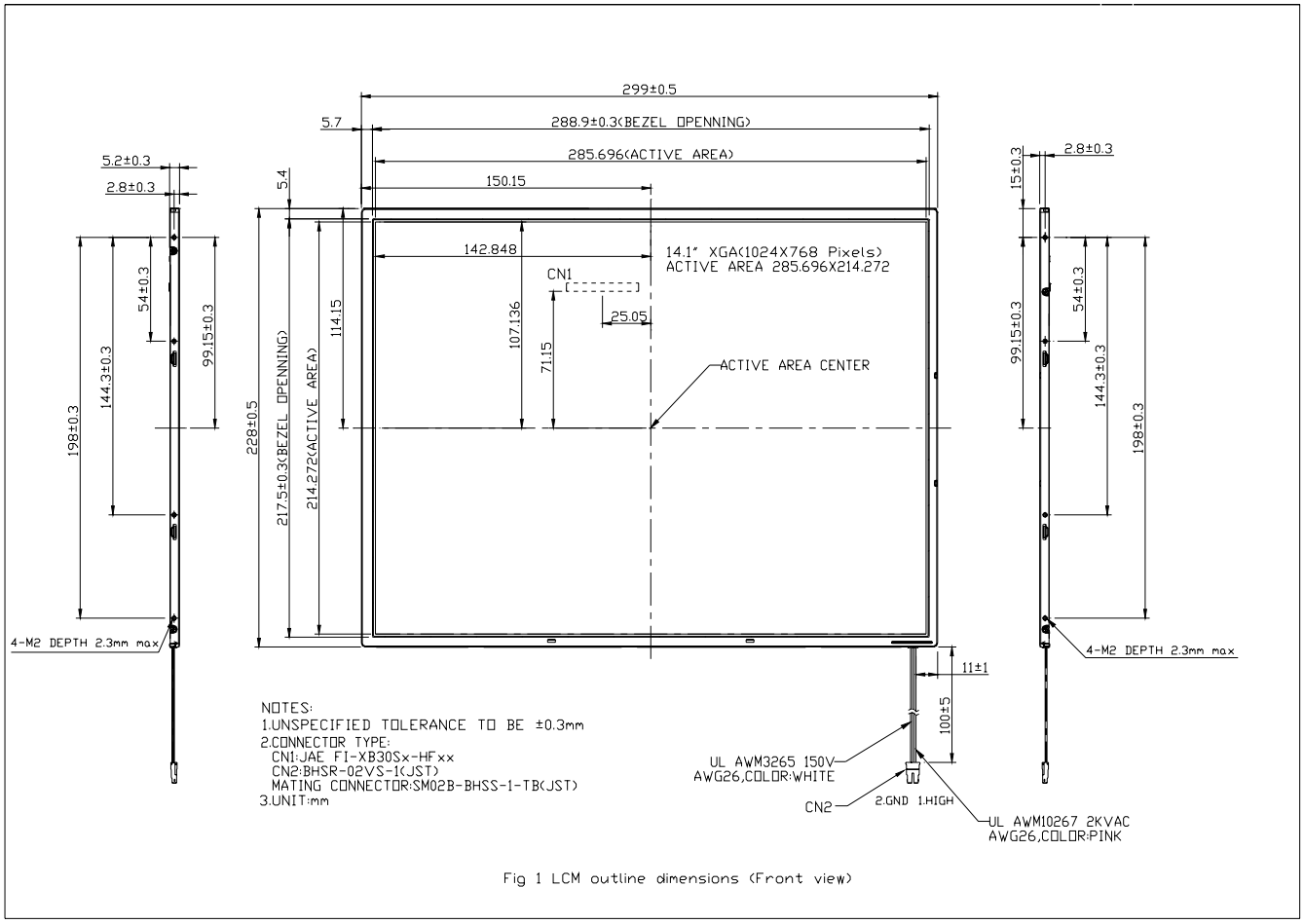


Fig 1 LCM outline dimensions (Front view)

13.2 LCM Outline Dimension (Rear View)

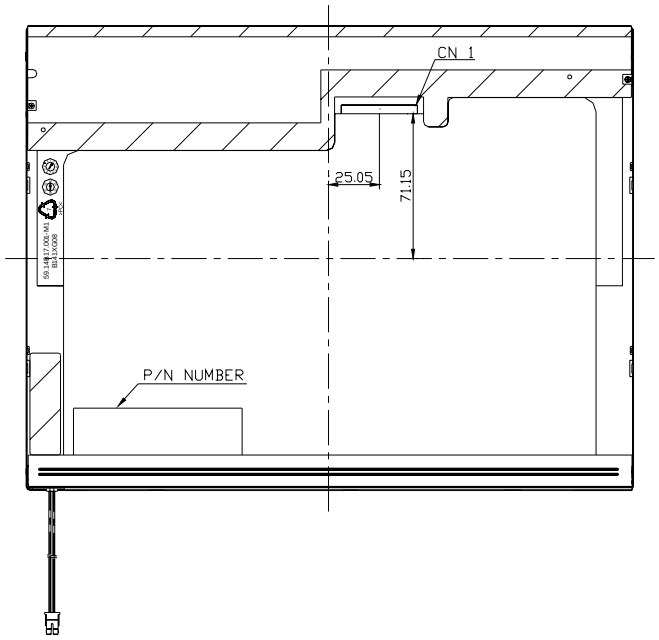


Fig 2 LCM outline dimensions (Rear view)

13.3 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.5 mm (See drawing)
Screw hole center location, from front surface = 2.8 ± 0.3mm (See drawing)
Screw maximum length = 2.3 mm (See drawing)
Screw Torque: Maximum2.5 kgzf-cm